REMARKS

Claims 1-13 and 27-34 have been examined. With this amendment, Applicant adds claims 35-38. Claims 1-13 and 27-38 are all the claims pending in the application.

I. Formalities

Applicant thanks the Examiner for acknowledging Applicant's claim for foreign priority and for confirming receipt of the certified copies of the priority documents filed on July 23, 2001.

II. Claim Rejections - 35 U.S.C. § 102

The Examiner has rejected claims 1-6, 9-11, 31 and 34 under 35 U.S.C. § 102(b) as being anticipated by Tanimoto *et al.* (US 4,622,632) ["Tanimoto"]. For at least the following reasons, Applicant traverses the rejection.

Claim 1 recites an image processing method that comprises "selecting a particular drawing level from a plurality of drawing levels ... based on at least one of an amount of computation processing, an amount of data and a display resolution." The Examiner contends that Tanimoto discloses this feature. Specifically, the Examiner contends that pyramidal processing unit 103 provides a plurality of processors, each associated with a display resolution. The Examiner cites a section of Tanimoto that discloses the use of parallel processing at different levels to contend that the claimed selecting is disclosed by Tanimoto.

Tanimoto discloses a computer system for operating upon a pyramidal data structure (col. 1, lines 6-8). The computer system is designed to distinguish patterns on the basis of image information (col. 1, lines 15-18 and col. 33, lines 43-57). To test for a particular pattern that

matches a portion of an object to be identified, local and global transformations are executed simultaneously on selected data elements at different levels of resolution (col. 33, lines 51-57).

Since the selected data elements correspond to different levels of the pyramidal processing unit and parallel processing is performed on different levels simultaneously, Applicant submits that Tanimoto does not disclose or suggest selecting a particular drawing level since any selection of levels disclosed by Tanimoto is for a plurality of levels, not a particular level as set forth in claim 1.

In addition, to the extent Tanimoto may disclose selecting levels, the selection is based on data elements, not the claimed amount of computation processing, an amount of data and a display resolution. The fact that the pyramid levels may correspond to display resolutions is irrelevant since any selection of the levels only depends on the selected data elements, which are selected based on a pattern of an object to be identified. Accordingly, the claimed selection of a particular level based on an amount of computation processing, an amount of data and a display resolution is not disclosed or suggested by Tanimoto.

Further, claim 1 also recites "performing processing ... at a higher drawing level than said particular drawing level ... thereby forming image data at said higher drawing level." The Examiner again cites the section of Tanimoto that discloses the use of parallel processing at different levels to contend that the claimed performing processing is disclosed by Tanimoto.

Applicants submit that, at most, Tanimoto discloses that data, which has been processed by the pyramidal processing unit, may be transmitted to graphic displays (col. 6, lines 29-34). There is no disclosure or suggestion that the data is processed at a level higher than the level of

the selected data elements. In fact, Tanimoto suggests that the selected data elements are processed by the actual processors on the same level as the selected data elements (see col. 33, lines 51-56). Accordingly, Tanimoto does not disclose or suggest the claimed processing at a higher level and arguably teaches away from the claimed feature.

Finally, the Examiner relies on the disclosure in col. 33, lines 43 to 56, of Tanimoto to teach the claimed performing processing by said computer graphics algorithm at a higher drawing level than said particular drawing level which was selected from said plurality of drawing levels based on editing data and attached data. However, the Examiner reliance on the description of "the pattern input signals" in col. 33, line 45, as disclosing the claimed editing data and attached data is misplaced. Applicant submits that the cited portion of col. 33, lines 43 to 56, does not address selecting a higher drawing level based on the editing data and its attached data which are set when forming a computer graphics image at said particular drawing level, and forming an image data at the selected higher drawing level. Accordingly, Tanimoto does not disclose or suggest the claimed processing at a higher level for this additional reason.

Because claims 2-6, 9-11, 31 and 34 depend on claim 1, Applicant submits that these claims are patentable at least by virtue of their dependency on claim 1.

III. Claim Rejections - 35 U.S.C. § 103

The Examiner has rejected claims 7, 8, 13 and 32 under 35 U.S.C. § 103(a) as being unpatentable over Tanimoto in view of Norton *et al.* (US 5,488,713) ["Norton"]. For at least the following reasons, Applicant traverses the rejection.

The Examiner concedes that the claimed features of 7, 13 and 32 are not taught by Tanimoto but contends that Norton cures the deficiency. The Examiner contends that one skilled in the art would have been motivated to combine the references in order to provide accurate prediction of parallel processing times.

Norton relates to a program development techniques for computer systems employing a shared memory multiprocessors or symmetric multiprocessor (SMP) (col. 1, lines 10-13). Specifically, the invention simulates execution times for an SMP program that is being developed by using a scheduler on a single processor workstation (col. 1, lines 19-55, col. 2, lines 11-16 and lines 27-37). Developing the applications on a single processor workstation allows the SMP system to be free from developing programs (col. 1, lines 22-24).

Accordingly, incorporating the invention of Norton into the parallel processing unit of Tanimoto as suggested by the Examiner would defeat the entire purpose of the invention in Norton since the applications would then have to be developed on the parallel processing unit of Tanimoto. Because Norton explicitly teaches away from a combination with Tanimoto, the Examiner's proffered reason for combining is not supported in the prior art.

In addition, Applicant submits that the invention in Norton is essentially a software implementation of a technique for evaluating program performance. Accordingly, the combination with Tanimoto would not cure the deficient teachings with respect to the claimed elements. For example, Tanimoto and Norton (taken alone or in combination) would still not provide the claimed second image processor with a different timing as set forth in claim 7 since Norton does not disclose or suggest adding additional hardware to a multiprocessor system.

Even if Norton's single processor host was incorporated into Tanimoto's pyramidal processing unit, there still is no disclosure or suggestion in either reference that any of the parallel processing of the selected data elements in Tanimoto can be performed on the single processor host at a different timing than the pyramidal processing unit. The Examiner's reliance on Fig. 3 for disclosing different timings is misplaced since it merely represents actual and simulated program execution times on the host processor (col. 7, lines 49-51). There is no disclosure or suggestion in Norton that its host processor can be combined with a parallel processing unit to perform actual graphics processing at a different timing.

The Examiner has rejected claims 12, 27-30 and 33 under 35 U.S.C. § 103(a) as being unpatentable over Tanimoto in view of Buytaert *et al.*(US 6,041,135) ["Buytaert"]. For at least the following reason, Applicant traverses the rejection.

Because Buytaert does not cure the deficient teachings of Tanimoto with respect to claim 1, Applicant submits that claims 12, 27-30 and 33 are patentable at least by virtue of their dependency on claim 1.

IV. New Claims

With this Amendment, Applicant adds claims 35-38. Applicant submits that these claims are patentable at least by virtue of their dependency on claim 1, as well as the feature set forth therein.

V. Conclusion

In view of the above, reconsideration and allowance of this application are now believed to be in order, and such actions are hereby solicited. If any points remain in issue which the

Examiner feels may be best resolved through a personal or telephone interview, the Examiner is kindly requested to contact the undersigned at the telephone number listed below.

The USPTO is directed and authorized to charge all required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account.

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